ALPHA DATA

ADM-XRC-7Z2
User Manual

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1 Overview

1.1 Introduction

The **ADM-XRC-7Z2** ("**7Z2**") is a high-performance Processor XMC for applications using Zynq-7000 SoCs from Xilinx.

1.2 Key Features

Key Features

- Single-width XMC, compliant to VITA Standard 42.0 and 42.3
- Zynq Z-7045 EPP in FFG900 package
- Processing System (PS) Block consisting of:
  - 1 bank of DDR3 SDRAM, 512MB
  - Quad SPI Flash memory, 512Mb
  - Removable Secure Digital (SD) Flash memory (Commercial Spec Option)
  - Ethernet interface to rear-panel P6 connector
  - Serial COM port connection to rear P6 connector
  - Two USB ports to rear P6 connector
  - One USB port to micro USB connector (Commercial Spec Option)
- Programmable Logic (PL) Block consisting of:
  - 2 banks of DDR3 SDRAM, 256MB per bank
  - Ethernet interface to rear-panel P6 connector
  - Serial COM port connection to rear P6 connector
  - Optional single-channel, dual-redundant MIL-STD-1553 Bus interface to P6 connector
  - 32 GPIO to P6 connector, 3.3V compatible, configurable as single-ended or differential signals
  - 20 GPIO to P6 connector, 3.3V, single-ended
- XMC Rear IO Interface P5:
  - VITA 42.3 Pinout
  - 8 HSSIO links to FPGA for PCI Express or user defined interface
  - PCI Express reference clock input
- XMC Rear IO Interface P6:
  - Two Gigabit Ethernet interfaces
  - Two USB Ports
  - Two Serial COM ports
  - 52 GPIO (16 diff-pairs and 20 single-ended)
- Platform manager with system monitoring

1.3 Order Code

ADM-XRC-7Z2/z-y(b)(c)(a)(t)

Name	Symbol	Configurations
Kintex-7 Device	z	Z045 , Z100
Kintex-7 Speed	y	1 , 2 , 3
MIL-STD-1553	c	blank = no 1553 interface /B = 1553 Bus Interface Fitted
Cooling	c	blank = air cooled commercial /ACE = Extended air cooled commercial /AC1 = air cooled industrial /CC1 = conduction cooled industrial
Conformal Coating	a	blank = No Coating /A = Acrylic (Humiseal 1B31) /P = Polyurethane (Arathane 5750)
XMC Connector Type	t	blank = XMC (VITA 42) Connectors /X2 = XMC2 (VITA 61) Connectors

Table 1 : Build Options

1.4 References & Specifications

ANSI/VITA 42.0	*XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.3	*XMC PCI Express Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	*IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001 (R2005)	*Conduction Cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4

Table 2 : References

2 PCB Information

2.1 Physical Specifications

Form Factor	Single Width XMC
Length (conduction-cooled)	143.75 mm
Width	74.0 mm
Height	10.0 mm
Weight (conduction-cooled)	TBD

Table 3 : Physical Specifications

2.2 Motherboard / Carrier Requirements

The **7Z2** is a single width XMC.3 mezzanine with P5 and P6 connectors.

The **7Z2** is compatible with either 5V or 12V on the "VPWR" power rail.

The Primary XMC connector, P5, is compatible with the XMC.3 (VITA 42.3) specification for PCI Express applications.

The Secondary XMC connector, P6 is not compatible with XMC.3 or XMC.10 (GPIO). It is important to check compatibility prior to installation. If in doubt, please contact Alpha Data for assistance.

IMPORTANT
It is important to check compatibility with the carrier card prior to installation.
The Secondary XMC connector, P6 has +5V (power) -/+6V (serial port) levels. It is not compatible with XMC.3 or XMC.10 (GPIO). It must not be connected to the Alpha Data ADM-EMC-II or ADM-XMC-II carrier cards. Please contact Alpha Data for carrier card compatibility.

2.3 Power Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx™ power estimation tools to determine the exact current requirements for each power rail.

3 Installation

3.1 Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

3.2 Hardware Installation

3.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

3.2.2 Installation in ADC-XMC-Breakout Carrier

Note:
Note: This operation should only be performed while the ADC-XMC-Breakout carrier is not powered.

Ensure that the **ADC-XMC-Breakout** carrier is fitted with the **AD-BREAKOUT-7Z2** wiring adaptor.

The **7Z2** should be secured to the **ADC-XMC-Breakout** carrier using M2.5 screws in the four holes provided.

Refer to the **ADC-XMC-Breakout** carrier documentation for switch configurations.

4 Functional Description

4.1 Overview

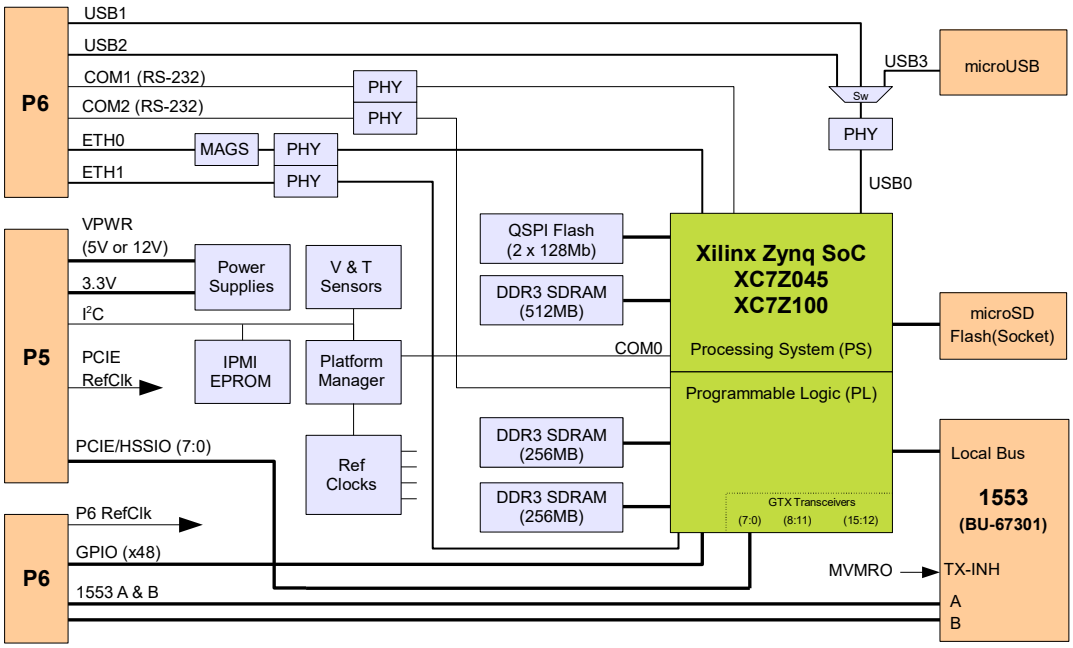

Figure 1 : ADM-XRC-7Z2 Block Diagram

4.1.1 Switch Definitions

There are two sets of 8-way DIP switches for configuring the board.

Their locations are shown in Figure 2

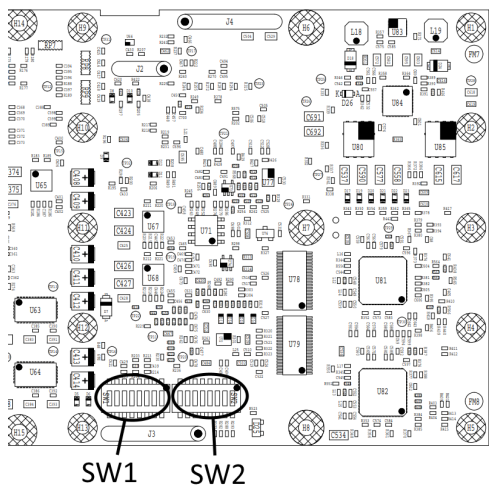

Figure 2 : DIP Switch Locations

Switch 1 Ref.	Function	OFF State	ON State
SW1-1	Reserved	-	-
SW1-2	Flash Boot Inhibit	Allow PS to boot PL from flash	Prohibit PS booting PL from flash
SW1-3	Systom Monitor Upgrade	Normal Operation	Reserved for factory use
SW1-4	Reserved	-	-
SW1-5	XMC JTAG	Isolate JTAG chain from P5	Connect JTAG chain to P5
SW1-6	Reserved	-	-
SW1-7	Reserved	-	-
SW1-8	BU JTAG En	Exclude BU67301 from JTAG chain	Include BU67301 in JTAG chain

Table 4 : Switch 1 Definitions

Switch 1 Ref.	Function	OFF State	ON State
SW2-1	BootSel 0	See Table 15	
SW2-2	BootSel 1	See Table 15	
SW2-3	Independent JTAG	Single (cascaded) JTAG chain at J4	Independent JTAG chains
SW2-4	PLL Bypass	PS PLL is used	PS PLL is bypassed
SW2-5	InhExtRst	Do not mask MRSTI	
SW2-6	Reserved	-	-
SW2-7	USB3 Mode	Zynq PS is USB Host and USB3 is downstream port	USB3 is OTG port
SW2-8	System Reset	Normal operation	PS System Reset

Table 5 : Switch 2 Definitions

4.1.2 LED Definitions

There are seven LEDs to provide a visual indication of the board status.

Their locations are shown in Figure 3

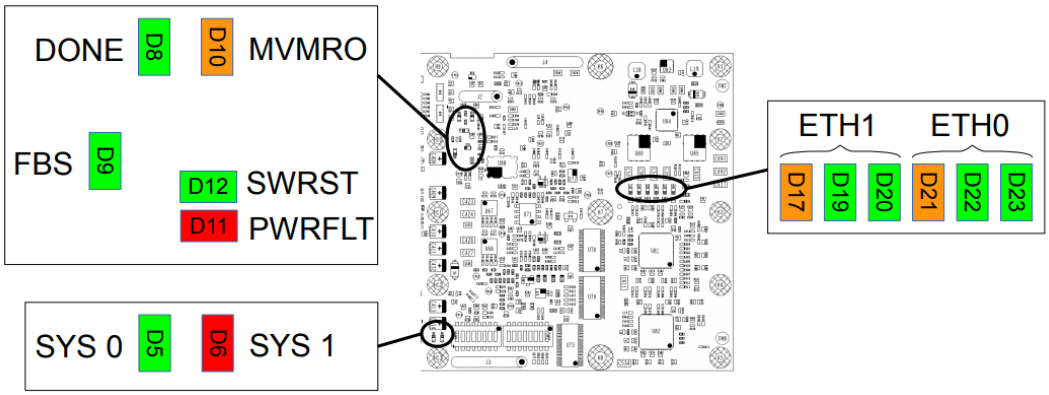

Figure 3 : LED Locations

Comp. Ref.	Function	ON State	Off State
D5 (Green)	System Monitor Status	See Table 19	
D6 (Red)	System Monitor Status	See Table 19	
D8 (Green)	FPGA (PL) Done	PL is configured	PL is not configured
D9 (Green)	Flash Boot Enable	Enable PS booting PL from flash	Disable PS booting PL from flash
D10 (Amber)	MVMRO	Enable writes to non-volatile memories	Inhibit writes to non-volatile memories
D11 (Red)	Power Good	Power Supplies off or faulty	Power Supplies operating correctly
D12 (Green)	System Reset	PS is in Reset	PS is not in Reset

Table 6 : Main LED Definitions

A further two sets of three LEDs provide an indication of the status of the two Ethernet interfaces

Comp. Ref.	Function	ON State	Off State
D23 (Green)	Ethernet 0 LED0	See Table 16	
D22 (Green)	Ethernet 0 LED1	See Table 16	
D21 (Amber)	Ethernet 0 LED2	See Table 16	
D20 (Green)	Ethernet 1 LED0	See Table 16	
D19 (Green)	Ethernet 1 LED1	See Table 16	
D17 (Amber)	Ethernet 1 LED2	See Table 16	

Table 7 : Ethernet LED Definitions

4.2 Primary XMC Connector P5

Full pinout information for this connector is listed in Table 20

4.2.1 XMC Platform Interface

4.2.1.1 IPMI I2C

A 2 Kbit I2C EEPROM (type M24C02) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

4.2.1.2 MBIST#

Built-In Self Test. This output signal is driven active (low) by the Zynq PS signal MIO9 (pin A24). It should be used to indicate that the board is performing self-test or that the Programmable Logic (PL) section of the SoC is unconfigured.

4.2.1.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. Amber LED D10 indicates a warning when this signal is not set and writes to non-volatile memory are enabled. The signal has a 100k pull-up resistor to assert it by default.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the Zynq PS at MIO50 (pin A19).

4.2.1.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier and should be used to reset any PCIE endpoint.

The MRSTI# signal is translated to 1.5V levels and connected to the Zynq PL at pin K2.

4.2.1.5 MRSTO#

XMC Reset Out. This optional output signal is connected to the Zynq PL at pin J4. It should only be driven when the board is connected to a master or Root Complex carrier slot.

4.2.1.6 MPRESENT#

Module Present. This output signal is connected directly to 0V.

4.2.1.7 JTAG

See Section Section 4.4

4.2.2 P5 HSSIO Links

Eight pairs of HSSIO links from the Zynq PL are routed to XMC connector P6.

The pinout and coupling of these links are compatible with PCI Express.

The Transmit (Tx) side of all eight lanes are AC coupled by 100nF capacitors, placed at the output from the PL.

The Receive (Rx) side of all eight lanes are directly connected from the connector to the PL.

Alternative coupling options are available as a special ordering option. Please contact Alpha Data for details.

4.3 Secondary XMC Connector P6

Full pinout information for this connector is listed in Table 21

4.4 JTAG Interfaces

4.4.1 On-board Interface

By default, the **7Z2** is configured to have a single (cascaded) JTAG scan chain connected to header J4. This allows the connection of the Xilinx JTAG cable for debug using the Xilinx ChipScope tools.

The board can also be set to have two independent scan chains using DIP switch SW2-3. (See Table 5. In independent mode, the main chain (with the Zynq PL, CPLD and XRM interface) is connected to J4, while the Zynq PS is connected to header J3.

If the cascaded or main scan chain is connected to the XMC connector (when SW1-5 is ON), header J4 should not be used.

4.4.2 XMC Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The interface can be connected to the cascaded or main interface (through level-translators) by switching SW1-5 ON. See Table 4

4.4.3 JTAG Voltages

The on-board JTAG scan chains uses 1.8V. The Vcc supply provided on J3 and J4 to the JTAG cable is +1.8V and is protected by a poly fuse rated at 350mA. 3.3V signals must not be used at header J3 or J4.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the XRM2 interface use the adjustable voltage XRM_VIO.

4.5 Clocks

The board has nine reference clocks: one from the carrier, and eight generated on-board.

The clocks MGTCLK250M, PROGCLK, REFCLK200M and ETH_CLK25M are generated by a single Silicon Labs Si5338B and are all synchronous.

Note:
Clock Termination
The LVDS clocks do not have termination resistors on the circuit board. On-die terminations in the FPGA must be enabled by setting the attribute "DIFF_TERM = TRUE". This can either be set in the source code when instantiating the buffer, or in the User Constraints File (UCF).

4.5.1 PCIe Reference Clock (PCIEREFCLK)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector, P5, at pins A19 and B19. This is connected to the Zynq PL via 10nF AC coupling capacitors. On the Zynq PL, it is connected to GTX Quad 112 to allow its use as reference for the eight GTX lanes on Quads 111 and 112.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK	MGTREFCLK0_112	HSCL	N8	N7

Table 8 : PCIEREFCLK Connections

4.5.2 MGTCLK250M

The fixed 250.0MHz reference clock, MGTCLK250M, is a differential clock signal using LVDS. It is connected to MGTREFCLK inputs on the Zynq PL at GTX Quad 111. (See Figure Figure MGT Links.)

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
MGTCLK250M	MGTREFCLK0_111	LVDS_25	U8	U7

Table 9 : MGTCLK250M Connections

4.5.3 PROGCLK

The programmable clock, PROGCLK, is a differential clock signal using LVDS. It is connected to MGTREFCLK inputs on the Zynq PL at GTX Quad 111. (See Figure Figure MGT Links.)

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK	MGTREFCLK1_111	LVDS_25	W8	W7

Table 10 : PROGCLK Connections

4.5.4 REFCLK200M

The fixed 200MHz reference clock, REFCLK200M, is a differential clock signal using LVDS. Three phase-matched copies are distributed to Global Clock inputs on the Zynq PL.

This clock can be used to generate application-specific clock frequencies using the PLLs within the Virtex-6 FPGA. It is also suitable as the reference clock for the IO delay control block (IDELAYCTRL) and memory interfaces.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK200M_A	IO_L13_MRCCC_10	LVDS_25	AG17	AG16
REFCLK200M_B	IO_L12_MRCC_33	SSTL15	G5	G4
REFCLK200M_C	IO_L13_MRCC_33	SSTL15	F5	E5

Table 11 : REFCLK200M Connections

4.5.5 PS_CLK33M3

The Zynq PS is provided with a 33.333MHz reference clock at the PS_CLK input on pin A22. This clock is asynchronous to the clocks generated by the Si5338B.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PS_CLK33M3	PS_CLK_500	LVCMOS18	A22	-

Table 12 : PS_CLK33M3 Connections

4.5.6 USB_REFCLK24M

The USB PHY and hub are provided with a 24.0MHz reference clock. This clock is asynchronous to the clocks generated by the Si5338B and is not connected to the Zynq SoC.

4.5.7 ETH_CLK25M

The Ethernet PHYs are provided with 25.0MHz reference clocks generated by the Si5338B. These are not connected to the Zynq SoC.

4.5.8 ETH1_CLK125M

The Ethernet PHY 1 generates a 125MHz reference clock that is connected to the Zynq PL at pin AF14.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
ETH1_CLK125M	IO_L12_MRCC_10	LVCMOS25	AF14	-

Table 13 : ETH1_CLK125M Connections

4.5.9 BU_REFCLK40M

The BU-67301 and Zynq PL are provided with a 40.0MHz reference clock. It is connected to the PL on clock-capable pin AE28. This clock is asynchronous to the clocks generated by the Si5338B.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
BU_REFCLK40M	IO_L13_MRCC_12	LVCMOS33	AE28	-

Table 14 : BU_REFCLK40M Connections

4.5.10 BU_HOST_CLK

In addition to the reference clocks, there is an additional clock, BU_HOST_CLK, used for the local bus interface between the Zynq PL and the BU-67301. Two phase-matched copies of BU_HOST_CLCK_OUT should be generated by the Zynq PL on pins AD25 and AE26.

BU_HOST_CLK_OUT_A on pin AD25 is connected to the HOST_CLK input on the BU-67301.

BU_HOST_CLK_OUT_B on pin AE26 is connected back in to the PL on pin AC28 as "BU_HOST_CLK".

4.6 Resets

The Zynq PS can be reset using the System Reset switch, SW2-8.

4.7 Zynq PS Block

4.7.1 Boot Modes

BootSel1 (SW2-2)	BootSel0 (SW2-1)	Boot Mode
OFF	OFF	JTAG
OFF	ON	Quad SPI
ON	OFF	SD Flash
ON	ON	Reserved

Table 15 : Boot Mode Selection

4.7.2 PS Memory Interfaces

4.7.2.1 Quad SPI Flash Memory

512Mb of QSPI flash memory (Micron N25Q256A11E1240E/MT41K128M16JT) is attached to the PS, and is used to store Zynq boot images, FPGA bitstreams and data.

4.7.2.2 MicroSD Flash Memory

An on-board microSD card holder is available to store Zynq boot images, FPGA bitstreams and data.

4.7.2.3 PS DDR3 Memory

The PS has one bank of DDR3 memory, constisting of 2 16-bit wide memory devices in parallel to provide a 32-bit datapath capable of running up to 533MHz (DDR-1066). 2Gb devices (Micron MT41K128M16JT-125) are fitted as standard to provide 512MB per bank.

4.7.3 Ethernet Interfaces

The **7Z2** has two Ethernet Interfaces at rear connector P6. Interface ETH0 is connected to the Zynq PS, while ETH1 is connected to the PL

Both interfaces have a Marvell 88E1512 PHY, connected to the Zynq via RGMII.

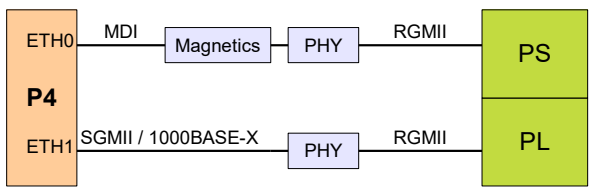

Figure 4 : Ethernet Interfaces

Each interface has three status LEDs. The functions of these are shown in Table 16below.

LED	Colour	Function
0	Green	
1	Green	
2	Amber	

Table 16 : Ethernet Status LEDs

4.7.4 Serial COM Ports

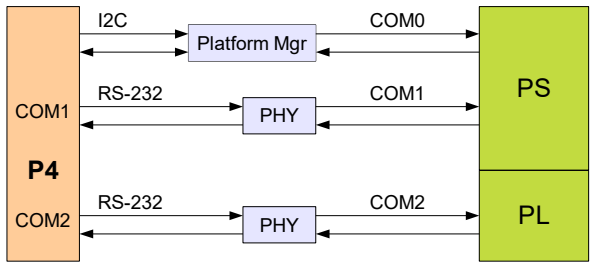

Figure 5 : Serial COM Ports

4.7.5 USB Interfaces

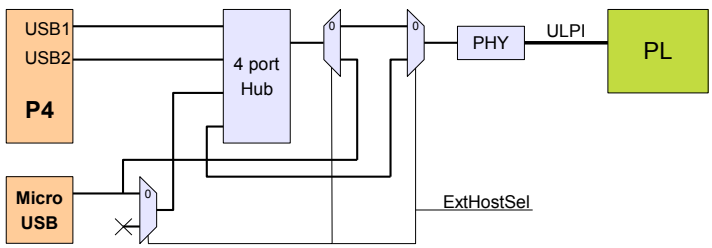

Figure 6 : USB Interfaces

4.8 Zynq PL Block

4.8.1 PL DDR3 Memory

The PL has two banks of DDR3 memory, each constisting of a single 16-bit wide memory device, capable of running up to 800MHz (DDR-1600). 2Gb devices (Micron MT41J64M16-187E) are fitted as standard to provide 256MB per bank.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). Full details of the interface, signaling standards are provided in the example design.

4.8.2 1553 Bus Controller

The PL is connected to a BU-67301B 1553 bus controller. The pinout is available in the example design.

4.8.3 Rear GPIO Interface

There are 20 single ended GPIO and 16 differential pairs connected to the P6 connector. The pinout is available in the example design.

4.9 System Monitoring

The **7Z2** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using an Atmel AVR microcontroller (uC).

The microcontroller continually measures all voltage rails and temperature sensors and transmits the results to the FPGA, where they are stored in blockram.

The following voltage rails and temperatures are monitored by the microcontroller:

Monitor	*Purpose*
VPWR	Board Input Supply (either 5.0V or 12.0V)
12V0	12V Board Input Supply
5V0	5V Board Input Supply
3V3	Board Input Supply
2V5	FPGA IO Supply
AUX_IO_2V0	FPGA Aux IO Supply
1V8	FPGA Aux Supply, Flash Memory
MGT_AUX_1V8	FPGA MGT Aux Supply
1V5	DDR3 SDRAM, Target FPGA memory I/O
1V0	FPGA Core Supply (VccINT)
MGT_1V2	FPGA MGT Vtt Supply
MGT_1V0	FPGA MGT Vcc Supply
3V3_INT	Internal 3.3V Supply
Temp1	microcontroller internal temperature
Temp2	TMP422 internal temperature
Temp3	FPGA on-die temperature (measured in TMP422)

Table 17 : Voltage and Temperature Monitors (in microcontroller)

The SDK includes an example application ("monitor") that reads the system monitor sensor values.

4.9.1 Automatic Temperature Monitoring

The system monitor checks that the board and FPGA are being operated within the specified limits. If the temperature is close to the limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the FPGA by asserting its "PROG" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in Table Temperature Limits. Note that the Min and Max values include a 5°C margin to prevent measurement errors triggering a false alarm.

	Target FPGA				Board (uC and PCB)			
	Min	Lower Warning	Upper Warning	Max	Min	Lower Warning	Upper Warning	Max
Commercial	-5°C	+5°C	+80°C	+90°C	-5°C	+5°C	+65°C	+75°C
Extended	-5°C	+5°C	+95°C	+105°C	-5°C	+5°C	+80°C	+90°C
Industrial	-45°C	-35°C	+95°C	+105°C	-45°C	-35°C	+80°C	+90°C

Table 18 : Temperature Limits

4.9.2 System Monitor Status LEDs

LEDs D5 (Green) and D6 (Red) indicate the microcontroller status.

LEDs	*Status*
Flashing Green + Flashing Red (alternate)	Service Mode
Red	Missing application firmware or invalid firmware
Red + Green	Standby (Powered off)
Green	Running and no alarms
Flashing Green + Red	Attention - alarm active
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Red	FPGA configuration cleared to protect board

Table 19 : System Monitor Status LEDs

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Appendix A: Rear Connector Pinouts

Appendix A.1: Primary XMC Connector, P5

	A	B	C	D	E	F
1:	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR(3)
2:	GND	GND	XMC_TRST#	GND	GND	MRSTI#
3:	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR(3)
4:	GND	GND	XMC_TCK	GND	GND	MRSTO#
5:	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR(3)
6:	GND	GND	XMC_TMS	GND	GND	+12V
7:	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR(3)
8:	GND	GND	XMC_TDI	GND	GND	-12V
9:	-	-	-	-	-	VPWR(3)
10:	GND	GND	XMC_TDO	GND	GND	GA0
11:	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR(3)
12:	GND	GND	GA1	GND	GND	MPRESENT#
13:	PER0p2	PER0n2	3.3V AUX(2)	PER0p3	PER0n3	VPWR(3)
14:	GND	GND	GA2	GND	GND	MSDA
15:	PER0p4	PER0n4	-	PER0p5	PER0n5	VPWR(3)
16:	GND	GND	MVMRO	GND	GND	MSCL
17:	PER0p6	PER0n6	-	PER0p7	PER0n7	-
18:	GND	GND	-	GND	GND	-
19:	REFCLK+0	REFCLK-0	-	WAKE#	ROOT0#	-
Notes:	(1) PCIe Channel Lanes (7:0) are directly connected to the Target FPGA.					
	(2) 3.3V AUX is required.					
	(3) VPWR can be either +5V or +12V.					

Table 20 : XMC Connector P5

Appendix A.2: Secondary XMC Connector, P6

	A	B	C	D	E	F
1:	ETH0_DB-	ETH0_DB+	GPIO_SE15	ETH0_DA-	ETH0_DA+	GPIO_SE14
2:	GND	GND	GPIO_13N	GND	GND	GPIO_12N
3:	ETH0_DD-	ETH0_DD+	GPIO_13P	ETH0_DC-	ETH0_DC+	GPIO_12P
4:	GND	GND	GPIO_11N	GND	GND	GPIO_10N
5:	GPIO_14N_CC	GPIO_14P_CC	GPIO_11P	GPIO_15N_CC	GPIO_15P_CC	GPIO_10P
6:	GND	GND	GPIO_9N	GND	GND	GPIO_8N
7:	GPIO_0N	GPIO_0P	GPIO_9P	GPIO_1N	GPIO_1P	GPIO_8P
8:	GND	GND	GPIO_SE8	GND	GND	GPIO_SE10
9:	GPIO_2N	GPIO_2P	GPIO_SE9	GPIO_3N	GPIO_3P	GPIO_SE11
10:	GND	GND	GPIO_SE4	GND	GND	GPIO_SE6
11:	ETH1_TxN	ETH1_TxP	GPIO_SE5	ETH1_RxN	ETH1_RxP	GPIO_SE7
12:	GND	GND	GPIO_SE1	GND	GND	GPIO_SE3
13:	A1553_N	A1553_P	GPIO_SE0	B1553_N	B1553_P	GPIO_SE2
14:	GND	GND	GPIO_SE16	GND	GND	GPIO_SE18
15:	GPIO_4N	GPIO_4P	GPIO_SE17	GPIO_5N	GPIO_5P	GPIO_SE19
16:	GND	GND	GPIO_SE13	GND	GND	USB1_VBUS
17:	GPIO_6N	GPIO_6P	GPIO_SE12	GPIO_7N	GPIO_7P	USB2_VBUS
18:	GND	GND	COM1_TXD	GND	GND	COM2_TXD
19:	USB1_DM	USB1_DP	COM1_RXD	USB2_DM	USB2_DP	COM2_RXD

Table 21 : XMC Connector P6

Revision History

Date	Revision	Nature of Change
4/03/14	0.1	First Draft
16/12/15	1.0	First Release
06/12/18	1.1	Updated to fill in some blank sections
24/02/20	1.2	Updated LED definitions with a diagram

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